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implanting an electrically neutral material into said substrate, wherein said electrically neutral material is implanted to a depth which is no greater than the depth of a diffusion region in said P-well.

REMARKS

In the February 26, 2002 Office Action, the Examiner has rejected claims 1-5 under the provisions of 35 U.S.C. §103(a) as being unpatentable over Abiko et al. (EP 0 880 174 A1) in further view of Gardner et al. (U.S. Patent No. 5,899,732). The Examiner has indicated that the subject matter of claim 7 is allowable over the prior art of record. Accordingly, claims 5 and 7 have been canceled and claim 1 has been amended to include all the limitations of dependent claims 5 and 7.

The Applicants have amended the claims of the present application to expedite the allowance of the application, but they reserve the right to file divisional applications directed to the subject matter of the originally filed claims including the claims which have been withdrawn from consideration.

The Applicants, therefore, respectfully submit that the amended claims are in condition for allowance, and the Examiner is requested to pass the present application to issue.

Respectfully submitted,

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Appendix

1. (Twice Amended) A method for fabricating radiation-tolerant integrated circuit devices, said method comprising:

depositing a layer of pad oxide on a semiconductor substrate;

selectively etching said pad oxide layer and said semiconductor substrate to define a trench within said semiconductor substrate;

implanting boron ions at an angle with respect to normal in said trench; [and]

implanting a p-type material to form a P-well having a depth greater than the depth of the trench; and

implanting an electrically neutral material into said substrate, wherein said electrically neutral material is implanted to a depth which is no greater than the depth of a diffusion region in said P-well.

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